08/712808

S P E C I F I C A T I O N

Docket No. 93-C-20C1

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN that we, Tsiu Chiu Chan and Frank Randolph Bryant, citizens of the United States of America, residing in the State of Texas, have invented new and useful improvements in a

STRUCTURE FOR TRANSISTOR DEVICES IN AN SRAM CELL

of which the following is a specification:

CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation in part of an application entitled "METHOD OF MAKING TRANSISTOR DEVICES IN AN SRAM CELL", Serial No. 08/390,117, filing date February 17, 1995, which is a divisional of Serial No. 08/159,462 filed November 30, 1993, now US 5426065.

Applicant incorporates said application Serial No. 08/159,462 by reference herein and claims the benefit of said application for all purposes pursuant to 37 C.F.R. § 1.78.

BACKGROUND OF THE INVENTION

1. **Field of the Invention:**

The present invention relates to integrated circuit devices and more specifically to field effect transistors (FET) for use in integrated circuits.

2. **Description of the Prior Art:**

Memories are devices that respond to operational orders, usually from a central processing unit. Memories may store large quantities of information in a digital format. In a memory system or unit, addresses are used to access the contents of the memory unit. A binary digit, also called a bit, is the basic information element stored in a memory unit. The smallest subdivision of a memory unit into which a bit of information can be stored is called a memory cell. A memory on a chip is physically arranged as a two-dimensional array of cells, wherein rows of cells are connected by row lines, also called word lines. A column of cells are connected by a column line, also called a bit line. These memory cells may be constructed by various configurations of transistors and/or capacitors.

A semiconductor memory is a memory that is implemented in a semiconductor material such as silicon. Metal-oxide

semiconductor (MOS) memories are common in the industry. A number of different types of MOS memories exist, such as a dynamic random access memory (DRAM) which is a metal oxide semiconductor memory that stores a bit of information as a charge on a capacitor, and a static random access memory (SRAM) which includes a bistable flipflop circuit requiring only a DC voltage applied to it to retain its memory. Normally, an SRAM contains four transistors plus either two transistors or two polysilicon load resistors as pull-up devices.

SRAMs have a disadvantage over a memory such as a DRAM. The components in an SRAM typically require the SRAM to have a larger basic cell than a DRAM. In SRAM memory cells, the data transfer gate transistor to pull-down transistor ON resistance ratio is typically required to be about 2.6x or greater to provide stability to the memory cell. Currently, the width of the pull-down transistor is required to be larger than the width of the transfer gate transistor to achieve the ratio requirement. This requirement places limitations on how small the memory cell may be made. Therefore, it would be desirable to have a transistor structure that would allow for a reduction in the area that a memory cell requires.

SUMMARY OF THE INVENTION

An SRAM memory cell having first and second transfer gate transistors. The first transfer gate transistor includes a first source/drain connected to a bit line and the second transfer gate transistor has a first source/drain connected to a complement bit line. Each transfer gate transistor has a gate connected to a word line. The SRAM memory cell also includes first and second pull-down transistors configured as a storage latch. The first pull-down transistor has a first source/drain connected to a second source/drain of said first transfer gate transistor; the second pull-down transistor has a first source/drain connected to a second source/drain of said second transfer gate transistor. Both first and second pull-down transistors have a second source/drain connected to a power supply voltage node. The first and second transfer gate transistors each include a gate oxide layer having a first thickness, and the first and second pull-down transistors each include a gate oxide layer having a second thickness, wherein the first thickness is different from the second thickness.

BRIEF DESCRIPTION OF THE DRAWINGS

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself however, as well as a preferred mode of use, and further objects and advantages thereof, will best be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1 is a schematic diagram of an SRAM cell in which a preferred embodiment of a present invention may be implemented;

Figure 2 is a layout of the SRAM cell depicted in Figure 1;

Figures 3A-3E are schematic cross-section views of a transfer gate transistor and pull-down transistor in an SRAM cell during processing; and

Figures 4-13 are layout diagrams of an SRAM during processing according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The process steps and structures described below do not form a complete process flow for manufacturing integrated circuits. The present invention can be practiced in conjunction with integrated circuit fabrication techniques currently used in the art, and only so much of the commonly practiced process steps are included as are necessary for an understanding of the present invention. The figures representing cross-sections and layouts of portions of an integrated circuit during fabrication are not drawn to scale, but instead are drawn so as to illustrate the important features of the invention.

Figure 1 is a schematic diagram of an SRAM cell **2** in which a preferred embodiment of the present invention may be implemented. SRAM cell **2** includes transistors **TG1**, **TG2**, **PD1**, and **PD2**. SRAM cell **2** also includes resistors **R1** and **R2**. Transistors **TG1** and **TG2** are transfer gate transistors in SRAM cell **2** while transistors **PD1** and **PD2** are pull-down transistors. Resistors **R1** and **R2** are used as pull-up devices.

Transistor **TG1** has a source/drain connected to bit line A, and transistor **TG2** has a source/drain connected to bit line B. Bit line B is a complement of bit line A. The gates of transistors **TG1** and **TG2** are connected to word line C. As can be seen, transistors **PD1** and **PD2** are connected in a cross-coupled configuration. In addition, the source/drain of transistor **TG1** and transistor **PD1** is connected to one end of resistor **R1** while the source/drain of transistor **PD2** and transistor **TG2** are connected to one end of resistor **R2**. The other ends of resistors **R1** and **R2** are connected to power supply voltage VCC while transistors **PD1** and **PD2** each have a source/drain connected to power supply voltage VSS.

Typically, the power supply voltage VCC is at a higher voltage than power supply voltage VSS. In a typical SRAM cell, transistors **PD1** and **PD2** typically have a width of 2.1μ and a length of 0.7μ. Transistors **PG1** and **PG2** typically have a width of 0.9μ and a length of 0.8μ.

Referring now to **Figure 2**, a layout of SRAM cell **2** from **Figure 1** is depicted. SRAM cell **2** in **Figure 2** includes word lines **6** and **8**, which are poly 1 lines. Bit lines **10** and **12** include bit line contacts **14a** and **14b**. In addition, SRAM cell **2** also has shared contacts **16a** and **16b**. Transistor **TG1** includes a gate **18**. Transistor **TG1** has a width W1 and a length L1. Similarly, transistor **TG2** has a gate **20** and a width W2 and a length L2. Pull-down transistor **PD1** includes gate **22** and has a width W3 and a length L3; pull-down transistor **PD2** includes gate **24** and has a width W4 and a length L4.

Figures 3A-3E are cross-section views of a transfer gate transistor and a pull-down transistor according to the present invention. Specifically, **Figure 3A** is a cross-section view of a pull-down transistor **26**, which includes a substrate **30** that is typically a monocrystalline silicon of a conventional crystal orientation known in the art. Many features of the present invention are applicable to devices employing semiconductor materials other than silicon as will be appreciated by those of ordinary skill in the art. Substrate **30** may be either a p-type substrate or an n-type substrate. In the present illustrative example, a p-type substrate is employed.

As can be seen in **Figure 3A**, a gate structure has been formed, which includes gate oxide layer **32** and polysilicon layer **34**. Source drain regions **36** have been implanted into substrate **30**. Various types of implants may be employed; for example, n-type impurities may be implanted into a p-type substrate. Source drain regions **36** are n-type active

regions in the illustrated example. Lightly doped drain (LDD) regions **38** are defined using sidewall oxide spacers **40** as known by those skilled in the art. Alternatively, LDDs **38** and sidewall spacers **40** may be omitted.

Transfer gate transistor **28** in **Figure 3B** is at the same processing step as pull-down transistor **26** in **Figure 3A**. After formation of the gate oxide **32** in **Figure 3A**, the region in which transfer gate transistor **28** is to be formed is masked off. Thus, no processing is performed in the region of transfer gate transistor **28** while the rest of pull-down transistor **26** is formed. As can be seen in this portion of SRAM cell **4**, a window **42** has been opened in dielectric layer **44** exposing gate oxide layer **32**. Dielectric layer **44** is an oxide in this example. Next, gate oxide layer **32** is etched away in **Figure 3C**, exposing surface **46** of substrate **30**. Thereafter, a new gate oxide layer **48** is grown on surface **46** of substrate **30** in window **42**, as shown in **Figure 3D**. This new gate oxide layer **48** preferably has a thickness less than that of the original gate oxide layer **32**.

Thereafter, the gate of pull-down transistor **28** is formed as illustrated in **Figure 3E**. The gate of pull-down transistor **28** includes gate oxide layer **48** and polysilicon layer **50**. Source/drains **52** also are implanted in substrate **30**. Source/drains **52** include LDDs **54**, which are again defined using sidewall oxide spacers **56**. The thickness of gate oxide **32** is greater than the thickness of gate oxide **48**. This type of processing is employed to create transfer gate transistors and pull-down transistors with different gate oxide thicknesses, which allows for a reduction in the width of pull-down transistors in an SRAM cell.

Although the depicted embodiment illustrates completely etching away the gate oxide of pull-down transistor **28**, then producing a gate oxide of the desired

thickness, other methods of producing different gate oxides may be employed according to the present invention. For example, a gate oxide layer may be grown for transfer gate transistor **28** first, and then an additional gate oxide layer can be grown on both pull-down transistor **26** and transfer gate transistor **28** to produce gate oxide layers of different thicknesses for each of the transistors. Transfer gate transistor **28** is completely masked from processing after completion, and remains in the form depicted in **Figure 3A** during the various processing steps applied to pull-down transistor **28** in **Figures 3B-3C**.

According to the present invention, a reduced width pull-down transistor dimension may be employed by adjusting the ratio of the gate oxide thickness between the transfer gate transistors and the pull-down transistors in the SRAM cell. The needed thicknesses of the two gate oxides may be selected using the following equation:

T90X

$$RATIO \leq \frac{Tox_{tg}}{Tox_{pd}} \frac{W_{pd}/L_{pd}}{W_{tg}/L_{tg}} \frac{Vcc-Vt_{tg}}{Vcc-Vt_{pd}}$$

where RATIO is the desired ratio of the transfer gate transistor and the pull-down transistor, Tox_{tg} is the gate oxide thickness of the transfer gate transistor, Tox_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is the width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, Vcc is the upper power supply voltage, Vt_{tg} is the threshold voltage of the transfer gate transistor, and Vt_{pd} is the threshold voltage of the pull-down transistor.

In the depicted example, RATIO is 2.6, VCC is equal to 3.3 volts, Vt_{tg} is 0.9 volts with a back bias, and Vt_{pd} is equal to 0.7 volts. If 0.5μ feature design rules are

utilized (L equal 0.5μ, W equal 0.6μ), the pull-down transistor width is 1.56μ. If the pull-down gate oxide thickness is 120Å, a 36% reduction in pull-down transistor width (1.0μ feature), will require a 134Å transfer gate oxide thickness. A 50% reduction in pull-down transistor width (0.8μ feature) requires a 165Å transfer gate oxide thickness. By reducing the width (W_{pd}) of the pull-down transistor, the overall area of SRAM cell may be reduced.

Figures 4-13 are layout diagrams of an SRAM cell during processing according to the present invention. In **Figure 4**, SRAM cell **4** located on a wafer has been processed and is ready for gate oxide. Active areas **100** have been formed in the substrate of the wafer by growing a field oxide everywhere else. Transfer gate oxide is grown on the wafer and a poly 1 is deposited. In **Figure 5**, the poly 1 is patterned for transfer gate transistors in areas **102**. Drain/source implantation for the transfer gate transistors is performed with resist patterns blocking implant into pull-down transistor areas **104** in **Figure 6**. Thereafter, a blanket threshold voltage adjust implant is performed for the pull-down transistors. Then undoped oxide is deposited on the wafer in a thickness of about 1000Å. The undoped oxide is removed in **Figure 7**. Undoped oxide in areas **106** are protected from removal with resist patterns to protect the poly 1, which causes only those areas **104** intended for the pull-down transistors to be exposed. The pull-down transistor gate oxide is grown; a thin buffer of poly is deposited in a layer of about 500Å. In **Figure 8**, resist patterns are utilized to open shared contacts in areas **108**. Then, poly plus polycide is deposited for poly 2.

In **Figure 9**, the poly 2 is patterned for pull-down transistors and the Vss line as shown in areas **110** in **Figure 9**. Drain/source implantation is then performed for the pull-down transistors. Thereafter, a thin oxide is deposited over the wafer in a layer of about 700Å. A spin-

on-glass process is performed to create a glass layer of about 700Å. This layer is cured and densified. Thereafter, thin glass is deposited on the wafer in a layer of about 700Å. In **Figure 10**, second shared contacts are opened using resist patterns to protect the rest of the SRAM cell from being opened. The second shared contacts are opened in areas **112**. Then, undoped poly 3 is deposited in a layer of about 700Å thick. In **Figure 11**, the poly 3 is patterned with resist to remain in areas **114**. This poly layer will be used for the SRAM cell pull-up resistors, and VCC supply lines. Undoped oxide is deposited in a layer of about 1000Å on the wafer and a blanket implant for poly 3 is performed to set the poly resistor resistance on the wafer. Thereafter, a n+ implant is performed for the VCC portions of poly 3 utilizing a resist pattern covering areas **116** in **Figure 12**. Contact windows are cut in areas **118** in **Figure 13**.

Thus, the present invention provides a method and structure for reducing the overall cell area of a memory cell. The present invention provides an ability to reduce the area of a memory cell by allowing the widths of the pull-down transistors to be reduced. The reduction in width is accomplished according to the present invention by selecting different gate oxide thicknesses for the pull-down transistor and the transfer gate transistor to maintain the desired ratio.

Although the depicted embodiment defines specific numbers for ratios, widths, lengths, in other parameters may be utilized by those of ordinary skill in the art following this disclosure. In addition, the different gate oxide thicknesses for transistors in the SRAM memory cell may be applied to other types of memory cells in which widths or lengths of transistors can affect the area that a cell requires.

While the invention has been particularly shown and described with reference to a preferred embodiment, it will be understood by those skilled in the art that various changes in form and detail may be made therein without departing from the spirit and scope of the invention.